“LOGIC FAMILY”

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INTRODUCTION

Logic family :-

- Various digital ICs available in market belong to various types. These types are known as "families".
- Based on the components and devices internally used, the digital IC families are named as RTL (Resistor Transistor Logic), TTL (Transistor Transistor Logic), DTL (Diode Transistor Logic), CMOS etc.

Classification of Logic Family :-

11.2.1 Classification Based on Devices Used :

- The two basic techniques for manufacturing ICs are:
  1. Bipolar technology
  2. Unipolar devices-Metal Oxide Semiconductor (MOS) technology.
- The classification of logic families is shown in Fig. 11.2.1.
Classification of logic family

Bipolar families:
- The bipolar families of logic circuits use the bipolar transistors fabricated on the chip. That means all the gates belonging to the bipolar family use the transistorised circuits.
- In the bipolar category there are three basic families called, Diode Transistor Logic (DTL), Transistor Transistor Logic (TTL) and Emitter Coupled Logic (ECL).
- DTL uses diodes and transistors, TTL uses transistors as the main elements. TTL has become the most popular family in SSI (Small Scale Integration) and MSI (Medium Scale Integration) chips, while ECL is the fastest logic family which is used for high speed applications.
- In the “Bipolar saturated” logic families, the bipolar transistors are used as the main device. It is used as a switch and operated in the saturation or cutoff regions.
- TTL is an example of saturated bipolar logic.
- In the unsaturated bipolar logic, the bipolar transistors are not driven into hard saturation. This increases the speed of operation. So the unsaturated bipolar ICs such as Schottky TTL and ECL (Emitter Coupled Logic) are much faster as compared to TTL.
- All these ICs are fabricated on silicon chips using different fabrication technologies.

Unipolar families:
- The MOS family use fabricates MOS Field Effect Transistors (MOSFETs) fabricated on the chip. So all the gates belonging to the MOS family use the MOSFET based circuits.
- In the MOS category there are three logic families namely PMOS (p-channel MOSFETs) family, NMOS (n-channel MOSFETs) family and CMOS (Complementary MOSFETs) family.
- PMOS is the oldest and slowest type. NMOS is used for the LSI (large scale integration) field i.e. for the microprocessors and memories.
- CMOS which uses a push pull arrangement of n-channel and p-channel MOSFETs, is extensively used where low power consumption is needed such as in pocket calculators.
11.3.1 Voltage and Current Parameters:

University Questions

Q. 1 Define the following terms and mention its standard values for TTL family:

1. Voltage and current parameter.
2. Power dissipation.
3. Noise margin.

(Dec. 13, 6 Marks)

Voltage parameters (Threshold levels):

- Ideally the input voltage levels of 0 V and +5 V (for TTL) are called as logic 0 and 1 levels respectively. However practically we won't always observe or obtain the voltage levels matching exactly to these values.
- Therefore it is necessary to define the worst case input voltages.

1. $V_{IL\,(\text{max})}$ - Worst case low level input voltage:
   This is the maximum value of input voltage which is to be considered as a logic 0 level. If the input voltage is higher than $V_{IL\,(\text{max})}$, then it will not be treated as a low (0) input level.

2. $V_{IH\,(\text{min})}$ - Worst case high level input voltage:
   This is the minimum value of the input voltage which is to be considered as a logic 1 level. If the input voltage is lower than $V_{IH\,(\text{min})}$, then it will not be treated as a High (1) input.

3. $V_{OH\,(\text{min})}$ - Worst case high level output voltage:
   This is the minimum value of the output voltage which will be considered as a logic HIGH (1) level. If the output voltage is lower than this level then it won't be treated as a HIGH (1) output.

4. $V_{OL\,(\text{max})}$ - Worst case low level output voltage:

Current parameters:

(a) $I_{IL}$ - Low level input current: It is the current that flows into the input terminals when a low level input voltage in the specified range is applied.

(b) $I_{IH}$ - High level input current: It is the current that flows into the input terminals when a high level input voltage in the specified range is applied.

(c) $I_{OL}$ - Low level output current: This is the current that flows out of the output when the output voltage happens to be in the specified low (0) voltage range and a specified load is applied.

(d) $I_{OH}$ - High level output current: This is the current flowing from the output when the output voltage happens to be in the specified HIGH (1) voltage range and a specified load is applied.
11.3.2 Fan-in and Fan-out:

**University Questions**

Q. 1 Explain fanout.

(Dec. 08, 2 Marks)

**Fan-in:** Fan-in is defined as the number of inputs a gate has. For example, a two input gate will have a fan-in equal to 2.

**Fan-out:** Fan-out is defined as the maximum number of inputs of the same IC family that a gate can drive without falling outside the specified output voltage limits. Higher fan-out indicates higher the current supplying capacity of a gate. For example, a fan out of 5 indicates that the gate can drive (supply current to) at the most 5 inputs of the same IC family.

11.3.3 Noise Margin:

Noise immunity is defined as the ability of a logic circuit to tolerate the noise without causing the output to change undesirably.

A quantitative measure of noise immunity of a logic family is known as noise margin.

**Propagation Delay (Speed of Operation):**

There is a time delay between these two time instants, which is called as the propagation delay.

Thus propagation delay is defined as time delay between the instant of application of an input pulse and the instant of occurrence of the corresponding output pulse. This is shown in

**Power Dissipation:**

Due to applied voltage and currents flowing through the logic ICs, some power will be dissipated in it, in the form of heat.

This power is in milliwatts. Care should be taken to reduce the power dissipation taking place in the logic IC in order to protect the IC against damage due to excessive temperature, to reduce the loading on power supplies etc.
Two Input TTL-NAND Gate (Totempole Output):

![C-1012] Fig. 11.4.2: Two input TTL NAND gate

A and B are the input terminals. The input voltages A and B can be either LOW (zero Volt ideally) or HIGH (+V_{cc} ideally).

1. **A and B both LOW**: If A and B both are connected to ground, then both the B-E junctions of transistor Q₁ are forward biased.
   - Hence diodes D₁ and D₂ in Fig. 11.4.3 will conduct to force the voltage at point C in Fig. 11.4.3 to 0.7 V.
   - This voltage is insufficient to forward bias base-emitter junction of Q₂ due to the presence of D₃. Hence Q₂ will remain OFF.
   - Therefore its collector voltage Vₓ rises to V_{cc}.
   - As transistor Q₃ is operating in the emitter follower mode, output Y will be pulled up to high voltage.

\[ Y = \begin{cases} 1 \text{ (HIGH)} & \text{For } A = B = 0 \text{ (LOW)} \\
\end{cases} \]

2. **Totempole output stage**

![C-1012] Fig. 11.4.3: Transistor Q₁ is replaced by its equivalent

Aforementioned transistor Q₁ by its equivalent.
3. **Either A or B LOW**: If any one input (A or B) is connected to ground with the other terminal left open or connected to $+V_{CC}$, then the corresponding diode ($D_1$ or $D_2$) will conduct.

- This will pull down the voltage at “C” to 0.7 V. (Fig. 11.4.3)
- This voltage is insufficient to turn ON $D_3$ and $Q_2$. So it remains OFF.
- So collector voltage $V_x$ of $Q_2$ will be equal to $V_{CC}$. This voltage acts as base voltage for $Q_3$.
- As $Q_3$ acts as an emitter follower, output $Y$ will be pulled to $V_{CC}$:
  \[
  Y = \begin{cases} 
  1 & \text{if } A = 0 \text{ and } B = 1 \\
  & \text{if } A = 1 \text{ and } B = 0
  \end{cases}
  \]
- The equivalent circuit for this mode is shown in Fig. 11.4.4(b).

---

(a) Equivalent circuit for $A = B = 0$

(b) Equivalent circuit for $A = 1$, $B = 0$
4. **A and B both HIGH**: If A and B both are connected to \(+ V_{cc}\), then both the diodes \(D_1\) and \(D_2\) will be reverse biased and do not conduct. Therefore voltage at point “C” i.e. at the anode of \(D_3\) increases to a sufficiently high value.

- Therefore diode \(D_3\) is forward biased and base current is supplied to transistor \(Q_2\) via \(R_1\) and \(D_3\) as shown in Fig. 11.4.4(c).
- As \(Q_2\) conducts, the voltage at \(X\) will drop down and \(Q_3\) will be OFF, whereas voltage at \(Z\) (across \(R_3\)) will increase to a sufficient level to turn ON \(Q_4\).
- As \(Q_4\) goes into saturation, the output voltage \(Y\) will be pulled down to a low voltage.

\[ Y = 0 \quad \text{...For} \quad A = B = 1 \]

- The equivalent circuit for this mode of operation is shown in Fig. 11.4.4(c).

(C-1014) **Fig. 11.4.4(c)**: Equivalent circuit for \(A = B = 1\)

- This discussion reveals that the circuit operates as a NAND gate.
Advantages of totem-pole output stage:

The advantages of using the totem-pole output stage are as follows:

1. With $Q_3$ in the circuit, the current flowing through $R_3$ will be equal to zero when the output $Y = 0$, power dissipation taking place in the circuit. That means when $Q_4$ is ON, as shown in Fig. 11.4.5(a). This is important because it reduces the power dissipation in $R_3$.

2. Another advantage of totem-pole arrangement is when the output $Y$ is HIGH. Here $Q_3$ is ON and $Q_4$ OFF, acting in the emitter follower mode. It will therefore have a very low output impedance (typically 10 $\Omega$). Therefore the output time constant will be very short for charging up any capacitive load on the output as shown in Fig. 11.4.5(b).

(a) No power dissipation in $R_3$  (b) Low output resistance

Disadvantages of Totem-pole output:

1. $Q_4$ in the totem-pole output turns OFF more slowly than $Q_3$ turns ON.
2. So before $Q_4$ is completely turned OFF, $Q_3$ will come into conduction. So for a very short duration of few nanoseconds, both the transistors will be simultaneously ON.
3. This is called as cross conduction and it will draw relatively large current (30 to 40 mA) from the 5 V supply.
The circuit diagram of a three input NAND gate is as shown in Fig. 11.5.2. Note that the multiple emitter transistor has three emitter terminals which act as the inputs A, B and C to the NAND gate.

(a) 

(b) Equivalent circuit of the multiple emitter transistor $Q_1$

(C-1685) Fig. 11.5.2 : Three input TTL NAND gate

The principle of operation of this circuit is exactly same as that of the two input NAND gate discussed in section 11.4.2.

If at least one of the inputs is low (0) then at least one of the diodes $D_1$, $D_2$, $D_3$ in Fig. 11.5.2(b) will be conducting. Hence the voltage at point C will be clamped to 0.7 V. Hence $Q_2$ will be off. So $Q_3$ will conduct and the output $Y = 1$ (HIGH).

$\therefore \quad Y = 1$ if at least one input is 0.
If \( A = B = C = 1 \) then \( D_1, D_2, D_3 \) will be off. So \( Q_2 \) will be turned on. So \( Q_3 \) will be turned off and \( Q_4 \) will be turned on. So the output \( Y = 0 \) (LOW).

\[
\therefore Y = 0 \text{ if all the inputs are 1.}
\]

Table 11.5.1 shows the truth table and the status of various transistors in the circuit.

**Table 11.5.1: Truth table of the 3-input NAND gate**

<table>
<thead>
<tr>
<th>Input</th>
<th>Status of various transistors</th>
<th>Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>( A )</td>
<td>( B )</td>
<td>( C )</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
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<tr>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>
Wired AND Connection (TTL):

If we connect the outputs of two gates directly to each other as shown in Fig. 11.6.1, then they are said to be wired ANDed with each other.

If the outputs are wired ANDed, then the final output is given by,

\[ Y = Y_1 \cdot Y_2 = (A \cdot B) \cdot (C \cdot D) = AB + CD \]

(a) Wired AND connection

(b) Wired AND connection with internal output stages shown

Can we wire AND the gates having Totempole output stage?

The answer is No. Wired AND connection should not be used for the totem-pole output circuits because of the current spike problem.

TTL circuits with open collector outputs are available which can be used for wired AND connection.
Why cannot we connect the totempole outputs together?

The outputs of two TTL gates with totem pole output are shown to be connected together in Fig. 11.6.2.

There are two reasons why such connection should be avoided.

Assume that output of Gate A is HIGH so $Q_{3A}$ is ON and output of Gate B is LOW so $Q_{4B}$ is conducting. Since both transistors operate in saturation, they are equivalent to small resistances. Hence $Q_{4B}$ acts as a very low resistive load and draws a very large current which is higher than its rated current.

Hence the transistor may get damaged due to overheating, after sometime.

Second problem caused by these high currents is that the current through $Q_{4B}$ will produce a voltage drop $V_{CE4B}$ to raise $V_{OL}$ between 0.5 to 1 V. This is greater than the allowable $V_{OL\text{(max)}}$. Due to these two reasons, the totempole outputs should never be directly connected together.
Open Collector Outputs (TTL):

We have seen that the gates having totem-pole output cannot be wired ANDed. Such a connection becomes possible if another type output stage called open collector output is used. The circuit diagram of a 2-input NAND gate is shown in Fig. 11.7.1. You will realize that this is the same TTL NAND gate which we have discussed earlier but with $R_3$ and $Q_3$ removed.

11.7.1 Disadvantages of Open Collector Output:

1. The value of pull up resistance is high (few kΩ). Therefore if the load capacitance is large then the RC time constant ($R_3C$) becomes large. This slows down the switching speed of $Q_4$. Therefore the gates having an open collector output will be slow.

Second disadvantage is increased power dissipation. When $Q_4$ is ON, a large current flows through the pull up $R_3$. Hence power dissipation is increased. This problem is eliminated if we use totem-pole output arrangement.
Operation:

1. With $A = B = 0$:
   - With $A = B = 0$, both the BE junctions of $Q_1$ are forward biased. So $Q_2$ remains OFF.
   - Hence no current flows through $R_1$. So $V_Z \approx 0$ V.
   - Therefore $Q_4$ is OFF and its collector voltage is equal to $V_{CC}$. So $Y = 1$ when $A = B = 0$.

2. With $A = 0$, $B = 1$ OR $A = 1$, $B = 0$:
   - One of the BE junctions is forward biased (the one corresponding to 0 input).
   - So $Q_2$ is OFF and $Q_4$ also is OFF. So its collector voltage is equal to $V_{CC}$.
   - Therefore output $Y = 1$ when any one input is low.

3. With $A = B = 1$:
   - When both the inputs are high, transistor $Q_1$ is turned OFF.
   - So $Q_2$ will be turned ON. Sufficient voltage is developed across $R_4$. Base current is applied to $Q_4$ and $Q_4$ goes into saturation.
   - So the output voltage is equal to $V_{CE\,(sat)}$ of $Q_4$ which is very small.
   - Thus $Y = 0$ when $A = B = 1$. The equivalent circuit for this mode is shown in Fig. 11.7.2.
## Difference between Totem-pole and Open Collector

<table>
<thead>
<tr>
<th>Sr. No.</th>
<th>Parameter</th>
<th>Totem-pole</th>
<th>Open collector</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.</td>
<td>Circuit components on the output side</td>
<td>$Q_3$ (pull up transistor), $D$ and $Q_4$ (pull down transistor) are used.</td>
<td>Only the pull down transistor $Q_4$ is used.</td>
</tr>
<tr>
<td>2.</td>
<td>Wired ANDing</td>
<td>Cannot be done</td>
<td>Easily be done</td>
</tr>
<tr>
<td>3.</td>
<td>External pull up resistor</td>
<td>Not required</td>
<td>Required to be connected.</td>
</tr>
<tr>
<td>4.</td>
<td>Power Dissipation</td>
<td>Low due to presence of pull up transistor $Q_3$.</td>
<td>High due to current flowing through $R_3$.</td>
</tr>
<tr>
<td>5.</td>
<td>Speed</td>
<td>Operating speed is high.</td>
<td>Operating speed is low.</td>
</tr>
</tbody>
</table>

---

### Tristate (Three state) TTL Devices:

It is called as tristate because it allows three possible output states namely:

1. **HIGH**
2. **LOW**
3. **High Impedance (Hi – Z) state.**
An additional input called Output Enable (OE) is introduced. Both the pull up and pull down transistors ($Q_3$ and $Q_4$) are being used.

The output stage block diagram of a tri-state inverter is shown in Fig. 11.8.1(a). The enable signal OE decides the operation of transistors $Q_3$ and $Q_4$.

When $OE = 1$, then the inverter operates as a normal inverter. If input is 0 then output will be 1 (HIGH) as shown in Fig. 11.8.1(a). The pull up transistor $Q_3$ will be ON.

Similarly with $OE = 1$ and input high (1), the output will be low because the pull down transistor $Q_4$ will be ON as shown in Fig. 11.8.1(b).

**High impedance state:**

- If the enable input $OE = 0$ (zero), then irrespective of the status of input, both the transistors will remain off as shown in Fig. 11.8.1(c).

- This state of operation is called as high impedance (Hi – Z) state. In this state the output terminal is essentially open circuit i.e. not connected anywhere.
CMOS inverter with positive input and output voltages is shown in Fig. 11.12.1(a).

(a) CMOS inverter with positive voltages

(b) Summary of operation

Operation:

1. With $V_i = 0$ Volt (logic 0):
   - With $V_i = 0$ Volt, the gate to source voltage $V_{GS}$ of $Q_1$ (NMOS) will be 0 Volt, hence it will be OFF. But $V_{GS}$ of $Q_2$ (PMOS) will be equal to $-V_{DD}$. So $Q_2$ will be ON.
   - Hence the output voltage will be equal to $+V_{DD}$ i.e. logic 1.

2. With $V_i = V_{DD}$ (logic 1):
   - With $V_i = +V_{DD}$, the gate to source voltages of the two MOSFETs are as follows:
     - $Q_1$ (NMOS): $V_{GS1} = V_{DD}$
     - $Q_2$ (PMOS): $V_{GS2} = 0$ Volt
   - Hence $Q_1$ will be turned ON and $Q_2$ will be OFF. So output gets connected to ground i.e. it will be “0”. Thus the inversion will take place.
   - The operation of this inverter has been summarized in Fig. 11.12.1(b).
Fig. 11.12.3 shows the CMOS 2-input NOR gate. It is obtained by modifying the CMOS inverter circuit.

(a) CMOS NOR gate

(b) Equivalent circuit

Q₁ and Q₂ are p-channel MOSFETs connected in series and Q₃, Q₄ are n-channel MOSFETs connected in parallel with each other.

Input A is connected to the gates of Q₁ and Q₃ while input B is connected to the gates of Q₂ and Q₄.

And output Y = 0 if Q₁ or Q₂ or Q₃, Q₄ both ON and Q₁, Q₂, Q₃, Q₄ both OFF. And output Y = 0 if Q₁ or Q₂ or Q₃, Q₄ both ON and Q₁, Q₂, Q₃, Q₄ both OFF.
1. With $A = B = 0$:
   - $V_{GS1} = -V_{DD}$, $V_{GS2} = -V_{DD}$. Hence $Q_1$ and $Q_2$ will be ON.
   - $V_{GS3} = 0$, $V_{GS4} = 0$. So $Q_3$ and $Q_4$ will be OFF.
   - The equivalent circuit for this mode is shown in Fig. 11.12.4(a) which shows that output $Y = V_{DD}$ (logical 1).
   - ∴ For $A = 0$, $B = 0$, output $Y = 1$.

2. With $A = 0$, $B = 1$:
   - If $A = 0$ and $B = 1$, then $Q_1$ will remain ON, but $Q_2$ will turn OFF.
   - $Q_3$ will remain OFF but $Q_4$ will be ON.
   - The equivalent circuit for this mode is shown in Fig. 11.12.4(b) which shows that output $Y = 0$ Volt (logical 0).
   - Thus $Y = 0$ for $A = 0$ and $B = 1$.

With $A = 1$, $B = 0$:
   - If $A = 1$ and $B = 0$ then $Q_1$ will be OFF and $Q_2$ will turn ON.
   - $Q_3$ will be turned ON but $Q_4$ will turn OFF.
   - Equivalent circuit of this mode is shown in Fig. 11.12.4(c) which shows that $Y = 0$ Volt (logical 0).
   - Thus $Y = 0$ for $A = 1$, $B = 0$.

For $A = B = 1$:
   - If $A$ and $B$ both are high (1), then $Q_1$ and $Q_2$ both will be OFF.
   - $Q_3$ and $Q_4$ both will be ON. Hence output $Y = 0$.
   - The equivalent circuit for this mode is shown in Fig. 11.12.4(d) and Table 11.12.1 summarizes the operation.
**Fig. 11.12.4(d)**: Equivalent circuit for $A = B = 1$

**Table 11.12.1: Summary of operation**

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Transistors</th>
<th>Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>$A$</td>
<td>$B$</td>
<td>$Q_1$</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>ON</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>ON</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>OFF</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>OFF</td>
</tr>
</tbody>
</table>
The two input CMOS NAND gate is shown in Fig. 11.12.5(a) and its equivalent circuit by replacing each MOSFET by a switch is shown in Fig. 11.12.5(b).

Q₁ and Q₂ are p-channel MOSFETs. They are connected in parallel with each other.

Q₃ and Q₄ are n-channel MOSFETs. They are connected in series with each other.

Input A is connected to gates of Q₁ and Q₃. So A controls the status of MOSFETs Q₁ and Q₃.

Input B is connected to gates of Q₂ and Q₄. So B controls the status of MOSFETs Q₂ and Q₄.
Operation:
1. \( A = B = 0 \):
   - With \( A = 0 \) and \( B = 0 \), both the PMOSFETs i.e. \( Q_1 \) and \( Q_2 \) will be ON. But both the
     N-MOSFETs i.e. \( Q_3 \) and \( Q_4 \) will be OFF.
   - As seen from the equivalent circuit of Fig. 11.12.6(a), the output \( Y = +V_{DD} \) (logic 1).
     So \( Y = 1 \) if \( A = B = 0 \)
2. With \( A = 0 \) and \( B = 1 \):
   - With \( A = 0 \) and \( B = 1 \), \( Q_1 \) will continue to be ON and \( Q_3 \) continues to be OFF. But \( Q_2 \) will
     now turn OFF and \( Q_4 \) will be turned ON.
   - The equivalent circuit of this mode is shown in Fig. 11.12.6(b) which shows that output
     \( Y = +V_{DD} \) i.e. logic 1. So \( Y = 1 \) if \( A = 0 \) and \( B = 1 \).
3. With \( A = 1 \) and \( B = 0 \):
   - With \( A = 1 \), \( Q_1 \) will be turned OFF and \( Q_3 \) will turn ON.
   - And with \( B = 0 \), \( Q_2 \) will be turned ON and \( Q_4 \) will be turned OFF.
   - As seen from the equivalent circuit of Fig. 11.12.6(c), the output \( Y = +V_{DD} \) (logic 1).
     So \( Y = 1 \) if \( A = 1 \) and \( B = 0 \).

(c-1059) Fig. 11.12.6 : Equivalent circuits

(c-1060) Fig. 11.12.6 : Equivalent circuit

(d) \( A = 1, B = 1 \)
With \( A = 1 \), \( B = 1 \):

- With \( A = B = 1 \) both P-MOSFETs i.e. \( Q_1 \) and \( Q_2 \) will be OFF and both the N-MOSFETs i.e. \( Q_3 \) and \( Q_4 \) will be ON.
- The equivalent circuit of this mode is shown in Fig. 11.12.6(d).
- It shows that output \( Y = 0 \) (LOW).
- So \( Y = 0 \) if \( A = B = 1 \).
- The operation of 2-input CMOS NAND gate is summarized in Table 11.12.2.

**Table 11.12.2: Summary of operation of a CMOS NAND gate**

<table>
<thead>
<tr>
<th>Inputs ( AB )</th>
<th>Transistors</th>
<th>Output Y</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 0</td>
<td>ON ON OFF OFF 1</td>
<td></td>
</tr>
<tr>
<td>0 1</td>
<td>ON OFF OFF 1</td>
<td></td>
</tr>
<tr>
<td>1 0</td>
<td>OFF ON ON 1</td>
<td></td>
</tr>
<tr>
<td>1 1</td>
<td>OFF OFF ON 0</td>
<td></td>
</tr>
</tbody>
</table>
### Comparison of CMOS and TTL

#### Table 11.1: Comparison of CMOS and TTL

<table>
<thead>
<tr>
<th>Sr. No.</th>
<th>Parameter</th>
<th>CMOS</th>
<th>TTL</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.</td>
<td>Device used</td>
<td>N-channel MOSFET and P-channel MOSFET</td>
<td>Bipolar junction transistor</td>
</tr>
<tr>
<td>2.</td>
<td>$V_{IH} \text{ (min)}$</td>
<td>3.5 V ($V_{DD} = 5$ V)</td>
<td>2 V</td>
</tr>
<tr>
<td>3.</td>
<td>$V_{IL} \text{ (max)}$</td>
<td>1.5 V</td>
<td>0.8 V</td>
</tr>
<tr>
<td>4.</td>
<td>$V_{OH} \text{ (min)}$</td>
<td>4.95 V</td>
<td>2.7 V</td>
</tr>
<tr>
<td>5.</td>
<td>$V_{OL} \text{ (max)}$</td>
<td>0.05 V</td>
<td>0.4 V</td>
</tr>
<tr>
<td>6.</td>
<td>High level noise margin</td>
<td>$V_{NH} = 1.45$ V</td>
<td>0.4 V</td>
</tr>
<tr>
<td>7.</td>
<td>Low level noise margin</td>
<td>$V_{NL} = 1.45$ V</td>
<td>0.4 V</td>
</tr>
<tr>
<td>8.</td>
<td>Noise immunity</td>
<td>Better than TTL</td>
<td>Less than CMOS</td>
</tr>
<tr>
<td>9.</td>
<td>Propagation delay</td>
<td>105 nS (Metal gate CMOS)</td>
<td>10 nS (Standard TTL)</td>
</tr>
<tr>
<td>10.</td>
<td>Switching speed</td>
<td>Less than TTL</td>
<td>Faster than CMOS</td>
</tr>
</tbody>
</table>

#### Table 11.2: Power dissipation per gate

<table>
<thead>
<tr>
<th>Sr. No.</th>
<th>Parameter</th>
<th>CMOS</th>
<th>TTL</th>
</tr>
</thead>
<tbody>
<tr>
<td>11.</td>
<td>Power dissipation per gate</td>
<td>$P_D = 0.1$ mW. Hence used for battery backup applications</td>
<td>10 mW</td>
</tr>
<tr>
<td>12.</td>
<td>Speed power product</td>
<td>10.5 pJ</td>
<td>100 pJ</td>
</tr>
<tr>
<td>13.</td>
<td>Dependence of $P_D$ on frequency</td>
<td>$P_D$ increases with increase in frequency.</td>
<td>$P_D$ does not depend on frequency.</td>
</tr>
<tr>
<td>14.</td>
<td>Fan out</td>
<td>Typically 50.</td>
<td>10</td>
</tr>
<tr>
<td>15.</td>
<td>Unconnected inputs</td>
<td>Unused inputs should be returned to GND or $V_{DD}$. They should never be left floating.</td>
<td>Inputs can remain floating. The floating inputs are treated as logic 1s.</td>
</tr>
<tr>
<td>16.</td>
<td>Component density</td>
<td>More than TTL since MOSFETs need smaller space while fabricating an IC.</td>
<td>Less than CMOS since BJT needs more space.</td>
</tr>
<tr>
<td>17.</td>
<td>Operating areas</td>
<td>MOSFETs are operated as switches, i.e. in the ohmic region or cut off region.</td>
<td>Transistors are operated in saturation or cut off regions.</td>
</tr>
<tr>
<td>18.</td>
<td>Power supply voltage</td>
<td>Flexible from 3 V to 15 V.</td>
<td>Fixed equal to 5 V.</td>
</tr>
</tbody>
</table>
Thank You